WHAT WE CLAIM IS:

1. A method of operation of a switching system, the switching system comprising:

a plurality of output stages each operable to supply packets of data to a respective output line;

a plurality of input stages each operable to receive packets of data on a respective input line, each received packet being destined for at least a respective one of the output stages; and

a transfer stage operable to transfer packets of data from any of the input stages to those of the output stages for which those packets are destined; and

the method of operation of the switching system comprising the steps of:

for each output stage, noting the temporal order in which the packets destined for that output stage are received by the input stages; and

controlling the transfer stage so that, for each output stage, the packets destined for that output stage are transferred from the input stages to that output stage in the noted order.

2. A method as claimed in claim 1, wherein:

the system operates according to time slots such that:

no more than one packet is received by each input stage during each time slot; and

no more than one packet is supplied by each output stage during each time slot; and

each time slot is divided into a plurality of phases such that:

no more than one packet is transferred from each input stage by the transfer stage during each phase; and

no more than one packet is transferred to each output stage by the transfer stage during each phase.

3. A method as claimed in claim 2, wherein each such time slot is divided into between two and four such phases.

4. A method as claimed in claim 2, wherein each such time slot is divided into four such phases.

5. A method as claimed in claim 2, wherein the controlling step includes the step, during each phase and for each output stage, of:

selecting that one of the input stages, if any, having that one of the packets which are destined for that output stage which is earliest in the noted temporal order; and

transferring that one packet from the selected input stage to that output stage unless there is input contention due to the selected input stage also having been selected for another of the output stages.

6. A method as claimed in claim 5, wherein the controlling step includes the step, if there is such input contention, of selecting that one of the output stages whose destined packet is earliest in the noted temporal order, unless there is none which is earliest.

7. A method as claimed in claim 6, wherein the controlling step includes the step, in the case of input contention, of repeating the controlling step for the or each output stage which is not selected in respect of the next earliest packet in the noted temporal order.

8. A method as claimed in claim 6, wherein the output stages have a predetermined ranking, and wherein the controlling step includes the step, if none of the packets is earliest as aforesaid, of selecting between the output stages in accordance with the predetermined ranking.

9. A method as claimed in claim 8, wherein the controlling step includes the step, in the case of input contention, of repeating the controlling step for the or each output stage which is not selected in respect of the next earliest packet in the noted temporal order.

10. A method as claimed in claim 1, wherein each input stage comprises a plurality of input buffers, one for each output stage, the method further including the step of placing each received packet in that one of the input buffers for the input line on which that packet is received and for the output stage for which that packet is destined.

11. A method as claimed in claim 1, wherein each output stage comprises a respective output buffer for the packets, and the packets are output from the respective output buffer to the respective output line in dependence upon the noted temporal order of the packets in the respective output buffer.

12. A switching system comprising:

a plurality of output stages each operable to supply packets of data to a respective

output line;

a plurality of input stages each operable to receive packets of data on a respective input line, each received packet being destined for at least a respective one of the output stages;

a transfer stage operable to transfer packets of data from any of the input stages to those of the output stages for which those packets are destined;

means for detecting, for each output stage, the temporal order in which the packets destined for that output stage are received by the input stages; and

means for controlling the transfer stage so that, for each output stage, the packets destined for that output stage are transferred from the input stages to that output stage in the detected temporal order.

13. A system as claimed in claim 12, wherein each output stage comprises a respective output buffer for the packets, and the packets are supplied from that buffer to the respective output line in dependence upon the detected temporal order of the packets in the respective output buffer.

14. A system as claimed in claim 12, wherein each input stage comprises an input buffer for each output stage.

15. A system as claimed in claim 14, wherein the input buffers are first-in-first-out buffers.

Page 74 of 95